NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

SEMESTER: VII

S. No	BoS	Sub Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	T.C.A.	ESE		
1	ETC	ET20711	Information Theory and Coding	3	1	-	20	15	15	50	70	120	4
2	ETC	ET2073X	Elective-3	3	1	-	20	15	15	50	70	120	4
3	ETC	ET2073X	Elective-4	3	1	-	20	15	15	50	70	120	4
4	ETC	ET20712	Telecom switching and cellular system	4	1	-	20	15	15	50	70	120	5
5	ETC	ET20721	Communication System Simulation Lab	-	-	3	30	-	-	30	20	50	2
6	ETC	ET20722	System design and simulation Lab	-	-	3	30	-	-	30	20	50	2
7	ETC	ET20723	Pract. Training	-	-	-	50	-	-	50	0	50	2
8	ETC	ET20724	Minor Project	-	-	12	100	-	-	100	50	150	6
9	ETC	ET20725	Seminar and Report Writing	-	-	2	50	-	-	50	0	50	1
			Total	13	4	20	340	60	60	460	370	830	30

ELECTIVE 3 (SEMESTER VII)

S. No.	BoS	Sub Code	Subject Name
1	ETC	ET20731	Digital signal processors and applications.
2	ETC	ET20732	ARM system architecture and design.
3	ETC	ET20733	Digital image processing.
4	ETC	ET20734	Digital communication hardware design.
5	ETC	ET20735	Nonlinear signal and image processing.
ELECTIVE 4 (SEMESTER VII)			
1	ETC	ET20736	Data Acquisition and computer interfacing
2	ETC	ET20737	Cryptography and network security
3	ETC	ET20738	Smart Antenna Systems
4	ETC	ET20739	Wireless Sensor Networks
5	ETC	ET20740	Analysis of Computer Communication Networks

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20711**
Subject: Information Theory and Coding
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Introduction to information theory; Probability, entropy and inference; Source coding theorem, symbol codes, stream codes, codes for integer.

UNIT II
Noisy channel coding: Dependent random variables, Communication over noisy channel, Noisy channel coding theorem, Error correcting codes and real channels.

UNIT III
Classical channel codes: Linear block codes, Cyclic codes, Convolutional codes, Maximum likelihood decoding of convolutional codes, Viterbi algorithm.

UNIT IV
Turbo codes: Design and construction, Performance, BCJR algorithm, applications.

UNIT V
Low density parity check codes: Representation of LDPC codes, Design and construction, Sum-product and message passing algorithm, Iterative decoder for LDPC codes, Low power and low complexity VLSI implementation.

Text Books:

1. Information Theory, Inference and Learning Algorithms, David MacKay, CUP, 2003.
2. Channel Codes – Classical and Modern, William Ryan, Shu Lin, CUP, 2009.
3. Communication Systems, Simon Haykin, Wiley India, 2001.

Reference Books:

1. Elements of Information Theory, M Cover, J A Thomas, Wiley India, 2006.
2. Information Theory and Network Coding, R W Yeung, Springer, 2008.
3. Coding and Information Theory, R W Hamming, Prentice Hall, USA, 1986.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20712**
Subject: Telecom Switching and Cellular System
Credits: 5
Total Theory Periods: 40 **Total Tutorial Periods: 10**

UNIT I
DIGITAL SWITCHING SYSTEMS: Introduction and history of telecom switching, Telephone equipment, Telephone exchange system, Switching functions, Space division switching, multiple stage switching, blocking probabilities, path finding, switch matrix control, Time division switching, Two dimensional switching, Digital cross connect systems.

UNIT II
GSM CELLULAR SYSTEM ARCHITECTURE: Cellular concept, Simplified design of classic cellular system, Basic GSM architecture, Basic radio transmission parameters of the GSM system, Logical channel description, GSM time hierarchy, GSM burst structures, Description of the call set-up procedure, Handover, Ensuring privacy and authentication of a user, Modifications and derivatives of GSM.

UNIT III
TRAFFIC ANALYSIS: Traffic characterization, arrival and holding time distributions, Loss systems, lost call cleared, returned, held, Network blocking probabilities, Delay systems. Traffic theory applied to cellular system, Ways of increasing system capacity, Channel assignment to the cells.

UNIT IV
SPEECH AND DATA IN GSM: Construction of a typical mobile station, Coding and decoding of speech signal, GMSK modulation, Sequential data detection. Data transmission in GSM, Data services in GSM, SMS, HSCSD, GPRS, EDGE.

UNIT V
TRANSMISSION SYSTEMS: Optical fiber transmission system elements, Line codes (mBnB code, Bit insertion code), DWDM, Pleciosynchronous digital hierarchy (PDH), Synchronous digital hierarchy (SDH), SONET multiplexing overview, Frame formats, operations, Payload framing and frequency justification, Virtual tributaries, E4 payload mapping, SONET optical standards, SONET network.

Text Books:

1. Digital Telephony, J C Bellamy, John Wiley and Sons.
2. Mobile communication systems, K Wesolowski, John Wiley and Sons, England 2002.

Reference Books:

1. Mobile cellular telecommunications, W C Y Lee, Tata McGraw-Hill, New Delhi 2006.
2. Telecommunication Switching & System, Thayagarajan V., Tata McGraw-Hill, New Delhi

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20721**
Subject: Communication System Simulation Laboratory
Credits: 2

Simulation experiments on digital communication, coding theory on platform like Matlab/Octave, Labview or C/C++. Set of 12 experiments as designed by the instructor.

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20722**
Subject: System Design and Simulation Laboratory
Credits: 2

Lab assignments given ET2073X Elective-3.

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20724**
Subject: Minor Project
Credits: 6

1. The students are expected to take up a Project under the guidance of a faculty from the Institute.
2. The topic of the project should be justified for the degree of B.Tech (Electronics & Telecommunication). The project chosen may have sufficient scope to be extended to Major project.
3. Students should submit synopsis of project within one month of offering of projects by faculty to the Student Projects Coordinator nominated by HoD. Synopsis should clearly state the quanta of work to be done in Minor project and the work for Major.
4. The students may be asked to work individually or in a group having not more than three students.
5. The quanta of work should justify a semester of work and live up to the standards of an NIT.
6. The students are expected to submit the report in standard format approved by the department in partial fulfillment of the requirement for the degree of B.Tech (Electronics & Telecommunication).
7. There will be a presentation cum viva-voce at the end of the semester and the students are to demonstrate the project at the time of viva-voce. The students will be evaluated for ESE in Minor project by a team of faculty nominated by the Head of Department.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20731**
Subject: Digital Signal Processor & Its Applications
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT II
EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, and Pipeline Programming models.

UNIT III
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS : Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS : The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing, FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the
TMS320C54XX, Computation of the signal spectrum.

UNIT V
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text Books:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataamani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing- A practical approach, Ifeachor & Jervis, Pearson Education.

Reference Books:

1. TMS320C50, TMS320C54XX, TMS320C6713 databooks.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20732**
Subject: ARM System Architecture and Design
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
ARCHITECTURAL FEATURES OF ARM PROCESSOR: Processor modes, Register organization, Exceptions and its handling, Memory and memory-mapped I/Os, ARM and THUMB instruction sets, addressing modes, ARM floating point architecture and DSP extensions, ARM co-processors.

UNIT II
ARM 9 TDMI ARCHITECTURAL STUDY: H/W architecture, Timing diagrams for various accesses, Memory buses: AMBA, ASB, APB, Case study of Intel Xscale architecture or Samsung ARM implementations

UNIT III
ARM AND THUMB INSTRUCTION SETS: Conditional execution and flags, Branch instructions, The barrel shifter, Immediate constants, Single register data transfer, Block data transfer, Stack management, Coprocessor instructions, Register access in Thumb, ARM architecture V5TE new instructions, Assembler workbooks
ARM / THUMB INTERWORKING: Switching between states, Branch exchange example, Mixing ARM and Thumb subroutines, ARM to thumb veneer, Thumb-to-ARM veneer, Interworking calls, and Interworking using codewarrior.

UNIT IV
ARM DEVELOPPER SUITE (ADS) OVERVIEW: Using the core tools, C/C++ compilers key features, Supplied libraries, Codewarrior introduction, Debugging with multi-ICE.
ADS INTRODUCTORY WORKBOOK: Compiling and running an example, Creating a header file, Creating a new project, Viewing registers and memory.
EXCEPTION HANDLING: Exception return instructions, Exception priority, Vector table instructions, Chaining exception handlers, Register usage in exception handlers, FIQ vs IRQ, Example C interrupt handler, Software managed interrupt controller, Issues when re-enabling interrupts, C nested interrupt example, Invoking SWIs, Data abort with memory management, The return address

UNIT V
EMBEDDED SOFWARE DEVELOPMENT: ROM or RAM at 0x0, ROM/RAM remapping, Exception vector table, Reset handler, Initialization : stack pointers, code and data areas, C library initialization, Scatter loading, Linker placement rules, Long branch veneers, C library functionality, Placing the stack and heap, Debugging ROM images.

Text Books:
1. ARM System Developer's Guide: Designing and Optimizing, Sloss Andrew N, Symes Dominic, Wright Chris, Morgan Kaufman Publication.
2. ARM System-on-Chip Architecture, Steven Furber, Pearson Education

Reference Books:
1. Technical references on www.arm.com.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20733**
Subject: Digital Image Processing
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Introduction to image processing: Applications and fields of image processing, Fundamental steps in Digital image processing, Elements of visual perception, Image sensing and acquisition, Basic Concepts in Sampling and Quantization, representing digital images

UNIT II
Image Enhancement in the Spatial Domain: Some basic gray level transformations, Histogram Processing, Histogram modification, Image subtraction, spatial filtering, Sharpening Spatial filters, use of first and second derivatives for enhancement ; Image Enhancement in the Frequency Domain, Gaussian filters, Homomorphic filtering Pseudocolouring : intensity slicing, gray level to color transformation,

UNIT III
Image Segmentation:-Some Basic Relationships between pixels, point, line and edge detection, Gradient operators, Canny edge detection, pyramid edge detection. Edge linking and boundary detection, Hough transform, Chain codes, boundary segments, skeletons, Boundary descriptors, Fourier descriptors.

UNIT IV
Thresholding: The role of illumination, global thresholding, adaptive thresholding, use of boundary characteristics for histogram improvement and local thresholding, Region based segmentation, Region growing, region splitting and merging.

UNIT V
Image Compression: Data redundancies Elements of information, variable-length coding, predictive coding, Transform coding, Image compression standards; Wavelets and Multiresolution processing: - Image pyramids, sub band coding
Basics of Image restoration, Color image processing Applications of Image Processing: - Finger print analysis, Digital watermarking, Optical character recognition etc.

Text Books:

1. Digital Image Processing, Gonzalez & Woods, Pearson Education, 2003
2. Introduction to Digital Image Processing, Alasdair Mc Andrew, Cengage learning, 2009
3. Fundamental of Digital Image Processing, A K Jain, PHI.

Reference Books:

1. Image Processing, Analysis and Machine Vision, Milan Sonka, Thomson Learning, 2001
2. Digital Image Processing, Pratt W.K, John Wiley & Sons, 2001

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20734**
Subject: Digital Communication Hardware Design
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Introduction to Virtex 2/4/6 board with RF transceivers (platform like WRAP, SMT349, Lyrtech SFF SDR etc), Architecture of Virtex 2/4/6 FPGA, RF module, Radio up and down converter modules, Timing module, Control register and other settings.

UNIT II
Programming with Virtex 4/6 FPGA, Programming with VHDL, Programming FPGA with Xilinx system generator and AccelDSP. Implementation of FIR and IIR filters on FPGA, Generation of sinusoid, Optimizing VHDL programs for FPGA architecture.

UNIT III
TRANSMITTER: Bandpass modulation, Binary ASK, BFSK, BPSK, QPSK generation with Virtex 6 board. Baseband pulse shaping to improve spectral efficiency, Sinc shaped pulse, Raised cosine pulse.

UNIT IV
RECEIVER DESIGN: Carrier phase recovery, Decision directed algorithm for phase recovery, Recursive Costas loop, Symbol timing recovery, Coherent detection of PSK, QPSK, Equalization, Implementation on FPGA board.

UNIT V
Non coherent receivers for ASK and FSK, Envelope detector. Implementation on a suitable software radio hardware.

Text Books:

1. Digital signal processing with field programmable gate arrays, 3/e, U Meyer-Baese, Springer India, 2007.
2. Communication systems- Analysis and design, H P E Stern, S A Mahmoud, Pearson Education India, 2004.
3. Transceiver and system design for digital communications, S R Bullock, Scitech Publishing 2000.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20735**
Subject: Nonlinear Signal and Image Processing
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
BASICS OF DISCRETE VOLTERRA SERIES: Introduction and basic definitions, nonlinear sampled-data systems, multidimensional z transform, discrete volterra series in the z domain, conditions for convergence and stability, matrix representation for multiple-input and multiple-output systems, nonlinear systems with fading memory, further considerations on fading memory, approximation of the system response by volterra series, discrete volterra series for binary signals, associated expansions and other approximations.

UNIT II
NONLINEAR ECHO CANCELLATION: Adaptive cancellers, nonlinear echo cancellation in data transmission, interleaved and passband nonlinear transversal filters.

UNIT III
KALMAN FILERING: Bayesian recursive relation and Kalman filter, Estimation of Gaussian random vectors, Extended Kalman filter, Unscented Kalman filtering.

UNIT IV
PERTICLE FILTERING: Bayesian inference in HMM, Sequential Monte Carlo methods, Basics of Monte Carlo method, Importance sampling, Particle filtering, SMC for filtering, Auxiliary particle filtering, Limitations of particle filter.

UNIT V
NONLINEAR IMAGE PROCESSING: Median and order statistics filter, Stack filters, Weighted median smoothers and filters, Spatial rank order selective filters, Nonlinear mean filters.

Text books:

1. Nonlinear aspects of telecommunications, A Boryz, CRC Press, 2001.
2. Nonlinear image processing, ed. S K Mitra, G L Sicuranza, Academic Press, USA 2001.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20736**
Subject: Data Acquisition and Computer Interfacing
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Bus system: Bus systems in microcomputers ST 100 bus, Multi bus, EISA, PCI Bus, HP IB/GPIB Bus, Bus and their applications. I/O Interface: Standard I/O interfaces RS-232 C, RS-232 D Centronics interface, current loop interface, and RS-449 communication interface. Programming for hardware in Visual Basic/Visual C++.

UNIT II
GPIB BUS: Bus structure, Signals, Controlling a device in GPIB, IEEE 488.2, SCPI. Plug-in boards and ISA, Description of ISA bus, Common interface chips, Interfacing to ISA. LabView PCI based data acquisition board operation.

UNIT III
OVERVIEW OF USB: Design goals of USB, Cables and connectors, LS/FS signalling environment, LS/FS transfer types and scheduling, Packets and transactions, Error recovery.

UNIT IV
HIGH SPEES USB OPERATION: Overview of HS device operation, HS signalling environment, Transfers, transactions and scheduling, HS error detection and handling, HS suspend and resume.

UNIT V
USB DEVICE CONFIGURATION: Configuration process, Hub configuration, Device classes, Overview of host software.

Text Books:

1. Visual basic for electronic engineering applications, V Himpe, Freely downloadable e-book.
2. USB system architecture, Don Anderson, Addison-Wesley Developer's Press, USA 2001.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20737**
Subject: Cryptography & Network Security
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
INTRODUCTION: OSI Security Architecture, Classical Encryption techniques, Cipher Principles, Data Encryption Standard – Block Cipher Design Principles and Modes of Operation - Evaluation criteria for AES – AES Cipher – Triple DES – Placement of Encryption Function – Traffic Confidentiality

UNIT II
PUBLIC KEY CRYPTOGRAPHY : Key Management - Diffie-Hellman key Exchange – Elliptic Curve Architecture and Cryptography - Introduction to Number Theory – Confidentiality using Symmetric Encryption – Public Key Cryptography and RSA.

UNIT III
AUTHENTICATION AND HASH FUNCTION: Authentication requirements – Authentication functions Message Authentication Codes – Hash Functions – Security of Hash Functions and MACs, MD5 message Digest algorithm, Secure Hash Algorithm, RIPEMD, HMAC Digital Signatures, Authentication Protocols – Digital Signature Standard.

UNIT IV
NETWORK SECURITY: Authentication Applications: Kerberos – X.509, Authentication Service, Electronic Mail Security – PGP – S/MIME - IP Security – Web Security.

UNIT V
SYSTEM LEVEL SECURITY: Intrusion detection – password management – Viruses and related Threats – Virus Counter measures – Firewall Design Principles – Trusted Systems.

Text Books:

1. Cryptography And Network Security – Principles and Practices, William Stallings, Prentice Hall of India, Third Edition, 2003.

Reference Books:

1. Network Security Private Communication in a public world, Charlie Kaufman, Radia Perlman & Mike Speciner, Prentice Hall of India Private Ltd., New Delhi.
2. Cryptography and Network Security, Atul Kahate, Tata McGraw-Hill, 2003.
3. Applied Cryptography, Bruce Schneier, John Wiley & Sons Inc, 2001.
4. Security in Computing, Third Edition, Charles B. Pfleeger, Shari Lawrence Pfleeger, Pearson Education, 2003.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code:ET20738**
Subject: Smart Antenna Systems
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Antenna arrays and diversity techniques, basic MIMO systems, channel model for multiple antenna systems.

UNIT II
Smart antenna introduction, smart antenna configuration, SDMA, architecture of smart antenna systems**.**

UNIT III
DOA(Direction of arrival) fundamentals ,DOA calculations, algorithms ESPIRIT,MUSIC.

UNIT IV
Beamforming fundamentals adaptive algorithms constant modulus, quasi Newton.

UNIT V
Space time processing, integration and simulation of smart antennas, smart antenna systems for mobile Adhoc networks.

Text Books:
1. Smart Antennas, Tapan k. Sarkar, IEEE Press Wiley Interscience

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20739**
Subject: Wireless Sensor Networks
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
Introduction to wireless sensor neteorks (WSN), Hardware of wireless sensor node, Network deployment, Localization, Coarse grained and fine grained localization, Network wide localization, Theoretical analysis of localization techniques.

UNIT II
Time synchronization, Traditional approaches, Fine grained clock synchronization, Coarse grained data synchronization. Medium access and sleep scheduling.

UNIT III
Sleep based topology control, Topologies for connectivity, topologies for coverage, Cross layer issues. Energy efficient and robust routing, Metric based approaches, Routing with diversity, Multipath routing, Energy aware routing.

UNIT IV
Distributed detection and estimation in sensor networks.

UNIT V
Data centric networking, Data centric routing, Data gathering with compression, Querying, Data centric storage and retrival.

Text Books:

1. Networking wireless sensor nodes, B Krishnamachari, Cambridge University Press, New York 2005.
2. Wireless sensor networks: An information processing approach, F Zhao, L J Guibas, Morgan Kaufman Publishers/ Elsevier, New Delhi 2004.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

Semester: 7 **Code: ET20740**
Subject: Analysis of Computer Communication Networks
Credits: 4
Total Theory Periods: 30 **Total Tutorial Periods: 10**

UNIT I
RANDOM PROCESS AND MARKOV CHAIN: Cross-Correlation Function, Covariance Function, CorrelationMatrix, Covariance Matrix, Markov Chains, Selection of the Time Step, Discrete-Time Markov Chains , Memoryless Property of Markov Chains , Markov Chain Transition Matrix, Markov Matrices, Diagonals of P, Eigenvalues and Eigenvectors of P, Constructing the State Transition Matrix P, Transient Behavior , Properties of $\mathbf{P}^n$, Finding s *(n)*. $\mathbf{P}^n$ Expressed in Jordan Canonic Form, Expressing P^n in Terms of Its Eigenvalues, Finding $\mathbf{P}^n$ Using the Z-Transform.

UNIT II
QUEUING ANALYSIS: Queue Throughput, Efficiency (η) or Access Probability (*p*a), Traffic Conservation, M/M/1 Queue, *M/M/*1 Queue Performance, M/M/1/B Queue, *M/M/*1*/B* Queue Performance, Performance Bounds on *M/M/*1*/B* Queue, *Mm/M/*1*/B* Queue, *Mm/M/*1*/B* Queue Performance, *M/Mm/*1*/B* Queue, *M/Mm/*1*/B* Queue Performance, *D/M/*1*/B* Queue, Performance of the *D/M/*1*/B* Queue, *M/D/*1*/B* Queue, Performance of the *M/D/*1*/B* Queue, Systems of communicating Markov Chains.

UNIT III
MODELING TRAFFIC FLOW CONTROL PROTOCOLS: Leaky Bucket Algorithm, Modeling the Leaky Bucket Algorithm, Single Arrival/Single Departure Model (*M/M/1 /B*), Leaky Bucket Performance (*M/M/1 /B* Case), Multiple Arrival/Single Departure Model (*Mm/M/1 /B*), Leaky Bucket Performance (*Mm/M/1 /B* Case), Token Bucket Algorithm, Modeling the Token Bucket Algorithm, Single Arrival/Single Departures Model (*M/M/1 /B*), Token Bucket Performance (*M/M/1 /B* Case), Multiple arrivals/Single Departures Model (*Mm/M/1 /B*), Token Bucket Performance (Multiple Arrival/Departure Case), Virtual Scheduling (VS) Algorithm, Modeling the VS Algorithm, VS Protocol Performance.

UNIT IV
MODELING ERROR CONTROL PROTOCOLS: Stop-and-Wait ARQ (SW ARQ) Protocol, Modeling Stop-and-Wait ARQ, SW ARQ Performance, Go-Back-*N* (GBN ARQ) Protocol, Modeling the GBN ARQ Protocol, Using Iterations to Find **s**, Algorithm for Finding s by Iterations, GBN ARQ Performance, Selective-Repeat (SR ARQ) Protocol, Modeling the SR ARQ Protocol, SR ARQ Performance.

UNIT V
MODELING MEDIUM ACCESS CONTROL PROTOCOLS: IEEE Standard 802.1p: Static Priority Protocol, Modeling the IEEE 802.1p: Static Priority Protocol, ALOHA, Modeling the ALOHA Network, ALOHA Performance, Slotted ALOHA, Modeling the Slotted ALOHA Network, Slotted ALOHA Performance, IEEE Standard 802.3 (CSMA/CD), IEEE 802.3 (CSMA/CD) Model Assumptions and performance, Carrier Sense Multiple Access-Collision Avoidance (CSMA/CA) performance, IEEE 802.11: DCF Function for Ad Hoc Wireless LANs, IEEE 802.11: DCF Medium Access Control, IEEE 802.11: DCF Model Assumptions, IEEE 802.11: DCF Protocol Performance.

Text Books:

1. Analysis of Computer and Communication Networks, Fayez Gebali, Springer, 2008.
2. Data Networks, D. P. Bertsekas, R. G. Gallager, 2nd Ed, Prentice Hall, 1992.